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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,853	02/09/2004	Gordon M. Grivna	ONS00470	7230
7590	12/28/2004		EXAMINER ABRAHAM, FETSUM	
Mr. Jerry Chroma Semiconductor Components Industries, L.L.C. Patent Administration Dept - MD/A700 P.O. Box 62890 Phoenix, AZ 85082-2890			ART UNIT	PAPER NUMBER
			2826	
			DATE MAILED: 12/28/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/773,853

Applicant(s)

GRIVNA, GORDON M.

Examiner

Fetsum Abraham

Art Unit

2826

An

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) all is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al (6,821,840).

As for claims 1,2,18,19, the prior art discloses an isolated device and a method of making the device whereby a semiconductor region (230) was provided composed of pluralities of shapes (elevated, trenched and depressed regions) in the semiconductor region and oxidizing the region with reactive species to form a low capacitance tub between a passive electrode (123) and the active portion of structure where a transistor is formed on. Although the prior art may not have used the specific terms used by applicant such as "low capacitance tub", it would have been obvious to one skilled in the art to conclude that the claimed structure is a duplicate of the prior art since low capacitance is the final product between the capacitive electrode and the active region due to the thick trench isolation element in between.

As for claims 3,20 the trench and region (220) form recessed portions of the structure and the oxidation process includes the entire semiconductor surface including the recessed portions.

As for claim 5, the electrode (123) represents the claimed capacitance over the isolation tub that comprises layers (221) and the trench isolation.

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As for claim 6, the step of forming the structure involving the etching of the semiconductor surface to form the recessed portions of the same.

As for claims 7,11,17 the depth and shape of any etched region in the art is variable that depends strictly on design choice. Furthermore, conductor spacing is a function of tolerated parasitic capacitance or anticipated capacitance as part of the overall system design.

As for claims 8,10,12-15, the capacitive electrode and the active region of the structure are freestanding with an offset in between. As for the claimed matrix, it is clear that semiconducting devices are formed in multiplicity by duplicating the same structure all over the substrate. Therefore, the concept of matrix is by default included in the prior art, and nearly continuous oxide layers were made by the process of oxidation to make the final isolation structures that include the trenches and the passive capacitive electrode on the isolation tub.

As for claim 9, the prior art substrate is silicon.

As for claim 16, there are sidewalls (224,234) associated with the overall structure. As for the claimed polysilicon being the material of choice for forming the passive or active elements, the material is known and common in the making of active or passive electrodes because it is as good a conductor as a metal. Clearly, a highly doped semiconductor materials, polysilicon and metal are the most common materials used in the art for the claimed elements.

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The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Refer to figure 4A of PN 6,180,995 and confirm that square shapes (40) are similar to the square shapes claimed in claim 17.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fetsum Abraham whose telephone number is: 571-272-1911. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915.

Fetsum Abraham

12/20/04